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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/635,006

08/06/2003

Koichi Fukuda

OKI.561

7606

20987

7590

12/23/2004

VOLENTINE FRANCOS, & WHITT PLLC  
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11951 FREEDOM DRIVE SUITE 1260  
RESTON, VA 20190

EXAMINER

HU, SHOUXIANG


ART UNIT

PAPER NUMBER

2811

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/635,006	FUKUDA, KOICHI	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 13 October 2004.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>5/27/04, 11/19/03</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election with traverse of Species I in the reply filed on October 13, 2004 is acknowledged. The traversal is on the ground(s) that claims 1-3, 5, 6, 13-15, 17 and 18 are generic to each of Species I-III. This is not found persuasive as explained below:

The Species I, II and III as identified in the previous office action are obviously mutually distinctive from each other. Although some of the pending claims may be readable on each of the species, it does not necessarily mean that these claims are each generic to the invention defined by each of the pending claims. For example, claim 1 defines raised S/D electrodes made of polysilicon, which may not necessarily be readable on the invention defined in claim 7 which recites raised S/D electrodes made of silicide.

Nevertheless, upon the allowance of any of the pending independent claims (1, 7 and 13, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of any of the allowed independent claims.

The requirement is still deemed proper and is therefore made FINAL.

***Claim Objections***

2. Claims 1-20 are objected to because of the following informalities and/or defects:

Claims 1, 7 and 13 each recites the subject matters that the recited thin silicon layer is surrounded by the recited isolation layer. However, according to the instant disclosure, especially the drawings, the thin silicon layer (33) is only sided, instead of being surrounded, by the recited isolation layer (37), as the term of "surround" may mean: to cover from all the directions.

In claims 2, 8 and 14, the term of "surrounds" appears to be inappropriate, as the sidewall does not fully surround the gate electrode.

Claims 5, 11 and 17 each recite the subject matters that the thin silicon layer is about 20 to 80 percent of a total thickness of it and the polysilicon or the silicide layer, which does not fully reflect what is disclosed in the specification (see page 7, lines 4-7), in which the total thickness includes each of the polysilicon layer, the silicide layer and the thin silicon layer.

In claims 6, 12 and 18, the term of "about less than" should read as: --less than about--.

Regarding claims 8 and 20, it is noted that only a portion of the recited silicide or conductive layer is formed on the gate electrode.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7-11, 13-17, 19 and 20, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 102(b) as being anticipated by Wakahara (JP 2000-183355; 06/30/2000; of record).

Wakahara discloses an SOI-MOS transistor (Fig. 11) which is naturally capable of functioning as a full depletion type as the SOI layer (3) therein can be as thin as 50 nm (see Paragraph 0020), comprising: a substrate (1); a BOX layer (2); the SOI layer (3) including a channel region and a source/drain region (9); an (element) isolation layer (4) siding the SOI layer on both of the two sides; a gate insulation layer (5); a gate electrode (6); a sidewall (11); and, a high mobility conductive layer including a silicon layer (13b) and/or a silicide layer (15), wherein the high mobility conductive layer is on, or extends to, the source/drain region, the gate electrode (6), the isolation layer (4) and the sidewall (11). It is noted that the silicon layer (13b) therein is naturally a polysilicon since the nature of the deposition in which at least a portion of the silicon layer (13b) is deposited on the isolation layer (4).

Regarding claims 5, 11 and 17, it is noted that thin silicon layer (3) in Wakahara is naturally about 20 to 80 percent of a total thickness of it, the polysilicon layer (13b) and the silicide layer (15), as shown in Figs. 10 and 11).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 6, 12 and 18, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Wakahara in view of Cheng (US 2002/0171107).

The disclosure of Wakahara is discussed as applied to claims 1-5, 7-11, 13-17, 19 and 20 above.

Although Wakahara does not expressly disclose that the thickness of the SOI layer (thin silicon layer) can be as thin as about 30 nm or less, it is art known that such thickness is well within the commonly recognized range for fully depletion type SOI layer for achieving desired good channel performance, as readily evidenced in the prior art such as Cheng (see Paragraph 0014).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to SOI device of Wakahara with the thickness of the SOI layer being less than about 30 nm, per the teachings of Cheng, so that a full depletion SOI-MOS transistor with desired good channel performance would be obtained.

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***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B-F are cited as being related to a raised S/D structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH

December 20, 2004



**SHOUXIANG HU  
PRIMARY EXAMINER**